

# TLV906x 10-MHz, RRIO, CMOS Operational Amplifiers for Cost-Sensitive Systems

## 1 Features

- Rail-to-Rail Input and Output
- Low Input Offset Voltage:  $\pm 0.3$  mV
- Unity-Gain Bandwidth: 10 MHz
- Low Broadband Noise:  $10 \text{ nV}/\sqrt{\text{Hz}}$
- Low Input Bias Current:  $0.5 \text{ pA}$
- Low Quiescent Current:  $538 \text{ }\mu\text{A}$
- Unity-Gain Stable
- Internal RFI and EMI Filter
- Operational at Supply Voltages as Low as  $1.8 \text{ V}$
- Easier to Stabilize with Higher Capacitive Load Due to Resistive Open-Loop Output Impedance
- Extended Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

## 2 Applications

- E-Bikes
- Smoke Detectors
- HVAC: Heating, Ventilating, and Air Conditioning
- Motor Control: AC Induction
- Refrigerators
- Wearable Devices
- Laptop Computers
- Washing Machines
- Sensor Signal Conditioning
- Power Modules
- Barcode Scanners
- Active Filters
- Low-Side Current Sensing

## 3 Description

The TLV9061 (single), TLV9062 (dual), and TLV9064 (quad) are single-, dual-, and quad- low-voltage ( $1.8 \text{ V}$  to  $5.5 \text{ V}$ ) operational amplifiers (op amps) with rail-to-rail input- and output-swing capabilities. These devices are highly cost-effective solutions for applications where low-voltage operation, a small footprint, and high capacitive load drive are required. Although the capacitive load drive of the TLV906x is  $100 \text{ pF}$ , the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler. These op amps are designed specifically for low-voltage operation ( $1.8 \text{ V}$  to  $5.5 \text{ V}$ ) with performance specifications similar to the OPAx316 and TLVx316 devices.

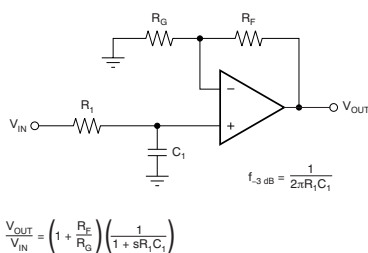
The TLV906x family helps simplify system design, because the family is unity-gain stable, integrates the RFI and EMI rejection filter and provides no phase reversal in overdrive condition.

### Device Information<sup>(1)</sup>

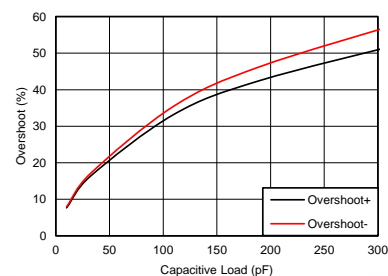
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV9061	SOT-23 (5)	$1.60 \text{ mm} \times 2.90 \text{ mm}$
	SC70 (5)	$1.25 \text{ mm} \times 2.00 \text{ mm}$
	SOT553 (5)	$1.65 \text{ mm} \times 1.20 \text{ mm}$
	X2SON (5)	$0.80 \text{ mm} \times 0.80 \text{ mm}$
	SOIC (8)	$3.91 \text{ mm} \times 4.90 \text{ mm}$
TLV9062	SOIC (8)	$3.91 \text{ mm} \times 4.90 \text{ mm}$
	TSSOP (8)	$3.00 \text{ mm} \times 4.40 \text{ mm}$
	VSSOP (8)	$3.00 \text{ mm} \times 3.00 \text{ mm}$
	VSSOP (10)	$3.00 \text{ mm} \times 3.00 \text{ mm}$
	WSON (8)	$2.00 \text{ mm} \times 2.00 \text{ mm}$
TLV9064	SOIC (14)	$8.65 \text{ mm} \times 3.91 \text{ mm}$
	TSSOP (14)	$4.40 \text{ mm} \times 5.00 \text{ mm}$
	WQFN (16)	$3.00 \text{ mm} \times 3.00 \text{ mm}$

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Single-Pole, Low-Pass Filter



### Small-Signal Overshoot vs Load Capacitance



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2017) to Revision C	Page
• Changed device status from Production Data/Mixed Status to Production Data .....	<b>1</b>
• Deleted package preview note from TLV9061 DPW (X2SON) package in <i>Device Information</i> table .....	<b>1</b>
• Deleted package preview note from TLV9061 DPW (X2SON) package pinout drawing .....	<b>4</b>
• Changed formatting of <i>ESD Ratings</i> table to show different results for all packages .....	<b>7</b>
• Deleted package preview note from DPW (X2SON) package in <i>Thermal Information: TLV9061</i> table .....	<b>7</b>

Changes from Revision A (June 2017) to Revision B	Page
• Added 8-pin PW package to <i>Pin Configuration and Functions</i> section .....	<b>5</b>
• Added DSG (WSO) package to <i>Thermal Information</i> table .....	<b>8</b>
• Added PW (TSSOP) to TLV9062 <i>Thermal Information</i> table .....	<b>8</b>
• Changed maximum input offset voltage value from $\pm 1.6$ mV to 2 mV .....	<b>9</b>
• Changed maximum input offset voltage value from $\pm 1.5$ to $\pm 1.6$ mV .....	<b>9</b>
• Changed minimum common-mode rejection ratio input voltage range from 86 dB to 80 dB .....	<b>9</b>
• Changed typical input current noise density value from 10 to 23 fA/ $\sqrt{\text{Hz}}$ .....	<b>9</b>
• Changed THD + N test conditions from $V_S = 5$ V to $V_S = 5.5$ V .....	<b>9</b>
• Added $V_{CM} = 2.5$ V test condition to THD + N parameter in <i>Electrical Characteristics</i> table .....	<b>9</b>
• Added maximum output voltage swing value from 25 mV to 60 mV .....	<b>9</b>
• Changed maximum output voltage swing value from 15 mV to 20 mV .....	<b>9</b>

## 5 Description (continued)

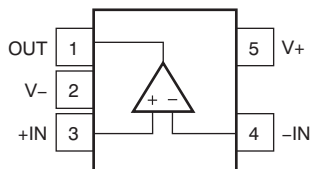
*Micro* size packages, such as SOT-553 and WSON, are offered for all the channel variants (single, dual and quad), along with industry-standard packages, such as SOIC, MSOP, SOT-23 and TSSOP.

## 6 Device Comparison Table

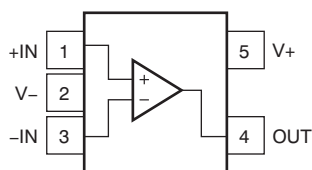
DEVICE	NO. OF CHANNELS	PACKAGE LEADS								
		DBV	DCK	DRL	DPW	D	DSG	DGK	PW	RTE
TLV9061	1	5	5	5	5	8	—	—	—	—
TLV9062	2	—	—	—	—	8	8	8	8	—
TLV9064	4	—	—	—	—	14	—	—	14	16

## 7 Pin Configuration and Functions

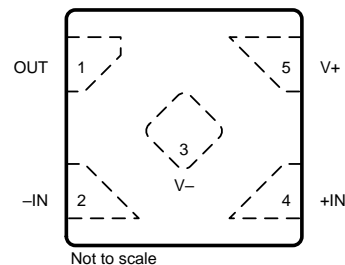
**TLV9061 DBV and DRL Package  
5-Pin SOT-23 and SOT-553  
Top View**



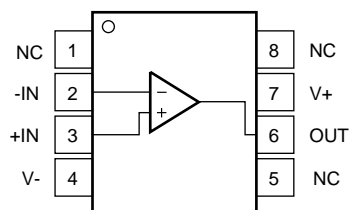
**TLV9061 DCK Package  
5-Pin SC70  
Top View**



**TLV9061 DPW Package  
5-Pin X2SON  
Top View**



**TLV9061 D Package  
8-Pin SOIC  
Top View**

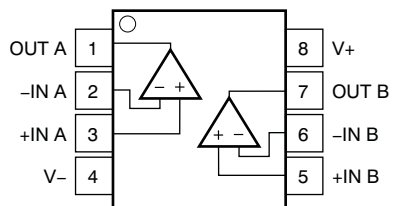


NC - No internal connection

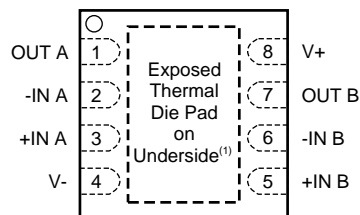
**Pin Functions: TLV9061**

NAME	PIN				I/O	DESCRIPTION
	DBV, DRL	DCK	D	DPW		
-IN	4	3	2	2	I	Inverting input
+IN	3	1	3	4	I	Noninverting input
OUT	1	4	6	1	O	Output
NC	—	—	1, 5, 8	—	—	No internal connection
V-	2	2	4	3	—	Negative (lowest) supply or ground (for single-supply operation)
V+	5	5	7	5	—	Positive (highest) supply

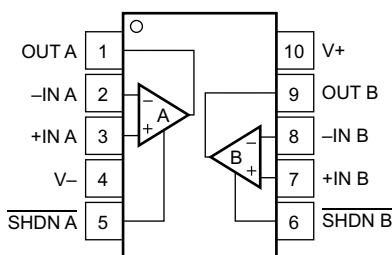
**TLV9062 D, DGK, PW Packages  
8-Pin SOIC, VSSOP, TSSOP  
Top View**



**TLV9062 DSG Package  
8-Pin WSON With Exposed Thermal Pad  
Top View**



**TLV9062 DGS Package  
10-Pin VSSOP  
Top View**



**Pin Functions: TLV9062**

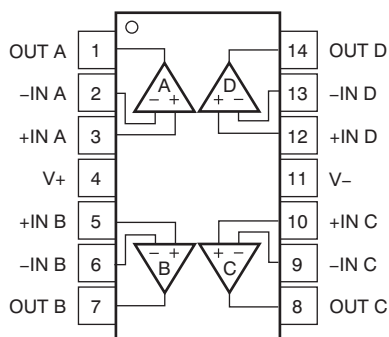
NAME	PIN		I/O	DESCRIPTION
	D, DGK, DSG, PW	DGS		
-IN A	2	2	I	Inverting input, channel A
+IN A	3	3	I	Noninverting input, channel A
-IN B	6	8	I	Inverting input, channel B
+IN B	5	7	I	Noninverting input, channel B
OUT A	1	1	O	Output, channel A
OUT B	7	9	O	Output, channel B
SHDN A	—	5	—	Shutdown (logic low), enable (logic high), channel A
SHDN B	—	6	—	Shutdown (logic low), enable (logic high), channel B
V-	4	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	10	—	Positive (highest) supply

**TLV9061, TLV9062, TLV9064**

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**TLV9064 D, PW Packages  
14-Pin SOIC, TSSOP  
Top View**



**Pin Functions: TLV9064**

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
-IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
-IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V-	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply

## 8 Specifications

### 8.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
Supply voltage			6		V
Signal input pins	Voltage <sup>(2)</sup>	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential	(V+) – (V–) + 0.2		
	Current <sup>(2)</sup>		–10	10	mA
Output short-circuit <sup>(3)</sup>			Continuous		mA
Temperature	Specified, T <sub>A</sub>		–40	125	°C
	Junction, T <sub>J</sub>		150		
	Storage, T <sub>stg</sub>		–65	150	

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

### 8.2 ESD Ratings

			VALUE	UNIT
TLV9061 DPW (X2SON) PACKAGE				
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>		±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>		±1500	
ALL OTHER PACKAGES				
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>		±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>		±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage	1.8	5.5	V
	Specified temperature	–40	125	°C

### 8.4 Thermal Information: TLV9061

THERMAL METRIC <sup>(1)</sup>		TLV9061			UNIT
		DBV (SOT-23)	DCK (SC70)	DPW (X2SON)	
		5 PINS	5 PINS	5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	221.7	263.3	467	°C/W
R <sub>θJC(top)</sub>	Junction-to-case(top) thermal resistance	144.7	75.5	211.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	49.7	51	332.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	26.1	1	29.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	49	50.3	330.6	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case(bottom) thermal resistance	N/A	N/A	125	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

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### 8.5 Thermal Information: TLV9062

THERMAL METRIC <sup>(1)</sup>		TLV9062				UNIT
		D (SOIC)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.6	201.2	94.4	205.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	104.6	85.7	116.5	106.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.7	122.9	61.3	133.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	55.6	21.2	13	34.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	99.2	121.4	61.7	132.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	34.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 8.6 Thermal Information: TLV9064

THERMAL METRIC <sup>(1)</sup>		TLV9064		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.8	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	64	64	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79	63	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	15.7	25.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	78.4	62.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.



## 8.7 Electrical Characteristics: $V_S$ (Total Supply Voltage) = $(V_+) - (V_-) = 1.8\text{ V to }5.5\text{ V}$

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V <sub>OS</sub>	Input offset voltage	V <sub>S</sub> = 5 V		±0.3	±1.6	mV
		V <sub>S</sub> = 5 V, T <sub>A</sub> = −40°C to +125°C			±2	
dV <sub>OS</sub> /dT	Drift	V <sub>S</sub> = 5 V, T <sub>A</sub> = −40°C to +125°C		±0.53		μV/°C
PSRR	Power-supply rejection ratio	V <sub>S</sub> = 1.8 V – 5.5 V, V <sub>CM</sub> = (V−)		±7	±80	μV/V
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V <sub>CM</sub>	Common-mode voltage range	V <sub>S</sub> = 1.8 V to 5.5 V	(V−) − 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V <sub>S</sub> = 5.5 V, (V−) − 0.1 V < V <sub>CM</sub> < (V+) − 1.4 V T <sub>A</sub> = −40°C to +125°C	80	103		dB
		V <sub>S</sub> = 5.5 V, V <sub>CM</sub> = −0.1 V to 5.6 V T <sub>A</sub> = −40°C to +125°C	57	87		
		V <sub>S</sub> = 1.8 V, (V−) − 0.1 V < V <sub>CM</sub> < (V+) − 1.4 V, T <sub>A</sub> = −40°C to +125°C		88		
		V <sub>S</sub> = 1.8 V, V <sub>CM</sub> = −0.1 V to 1.9 V T <sub>A</sub> = −40°C to +125°C		81		
INPUT BIAS CURRENT						
I <sub>B</sub>	Input bias current			±0.5		pA
I <sub>OS</sub>	Input offset current			±0.05		pA
NOISE						
E <sub>n</sub>	Input voltage noise (peak-to-peak)	V <sub>S</sub> = 5 V, f = 0.1 Hz to 10 Hz		4.77		μV <sub>PP</sub>
e <sub>n</sub>	Input voltage noise density	V <sub>S</sub> = 5 V, f = 10 kHz		10		nV/√Hz
		V <sub>S</sub> = 5 V, f = 1 kHz		16		nV/√Hz
i <sub>n</sub>	Input current noise density	f = 1 kHz		23		fA/√Hz
INPUT CAPACITANCE						
C <sub>ID</sub>	Differential			2		pF
C <sub>IC</sub>	Common-mode			4		pF
OPEN-LOOP GAIN						
A <sub>OL</sub>	Open-loop voltage gain	V <sub>S</sub> = 1.8 V, (V−) + 0.04 V < V <sub>O</sub> < (V+) − 0.04 V, R <sub>L</sub> = 10 kΩ		100		dB
		V <sub>S</sub> = 5.5 V, (V−) + 0.05 V < V <sub>O</sub> < (V+) − 0.05 V, R <sub>L</sub> = 10 kΩ	104	130		
		V <sub>S</sub> = 1.8 V, (V−) + 0.06 V < V <sub>O</sub> < (V+) − 0.06 V, R <sub>L</sub> = 2 kΩ		100		
		V <sub>S</sub> = 5.5 V, (V−) + 0.15 V < V <sub>O</sub> < (V+) − 0.15 V, R <sub>L</sub> = 2 kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V <sub>S</sub> = 5 V, G = +1		10		MHz
φ <sub>m</sub>	Phase margin	V <sub>S</sub> = 5 V, G = +1		55		°
SR	Slew rate	V <sub>S</sub> = 5 V, G = +1		6.5		V/μs
t <sub>S</sub>	Settling time	To 0.1%, V <sub>S</sub> = 5 V, 2-V step , G = +1, C <sub>L</sub> = 100 pF		0.5		μs
		To 0.01%, V <sub>S</sub> = 5 V, 2-V step, G = +1, C <sub>L</sub> = 100 pF		1		
t <sub>OR</sub>	Overload recovery time	V <sub>S</sub> = 5 V, V <sub>IN</sub> × gain > V <sub>S</sub>		0.2		μs
THD + N	Total harmonic distortion + noise <sup>(1)</sup>	V <sub>S</sub> = 5.5 V, V <sub>CM</sub> = 2.5 V, V <sub>O</sub> = 1 V <sub>RMS</sub> , G = +1, f = 1 kHz		0.0008%		
OUTPUT						
V <sub>O</sub>	Voltage output swing from supply rails	V <sub>S</sub> = 5.5 V, R <sub>L</sub> = 10 kΩ			20	mV
		V <sub>S</sub> = 5.5 V, R <sub>L</sub> = 2 kΩ			60	
I <sub>SC</sub>	Short-circuit current	V <sub>S</sub> = 5 V		±50		mA
Z <sub>O</sub>	Open-loop output impedance	V <sub>S</sub> = 5 V, f = 10 MHz		100		Ω
POWER SUPPLY						

(1) Third-order filter; bandwidth = 80 kHz at -3 dB.

**TLV9061, TLV9062, TLV9064**

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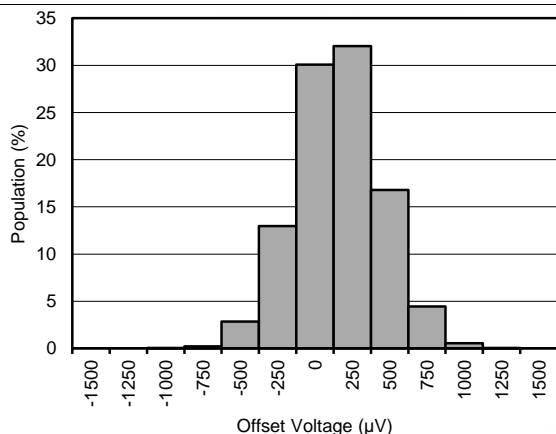
[www.ti.com](http://www.ti.com)
**Electrical Characteristics:  $V_S$  (Total Supply Voltage) =  $(V_+) - (V_-) = 1.8\text{ V to }5.5\text{ V}$  (continued)**

 at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

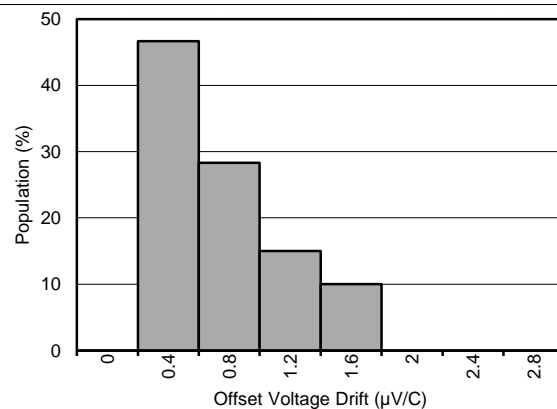
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_Q$ Quiescent current per amplifier	$V_S = 5.5\text{ V}$ , $I_O = 0\text{ mA}$		538	750	$\mu\text{A}$
	$V_S = 5.5\text{ V}$ , $I_O = 0\text{ mA}$ $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			800	

## 8.8 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

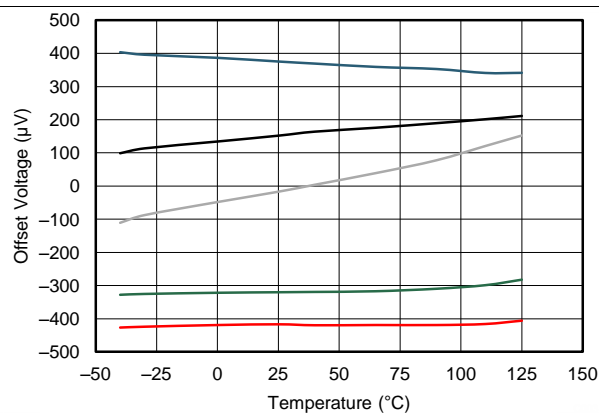


**Figure 1. Offset Voltage Production Distribution**

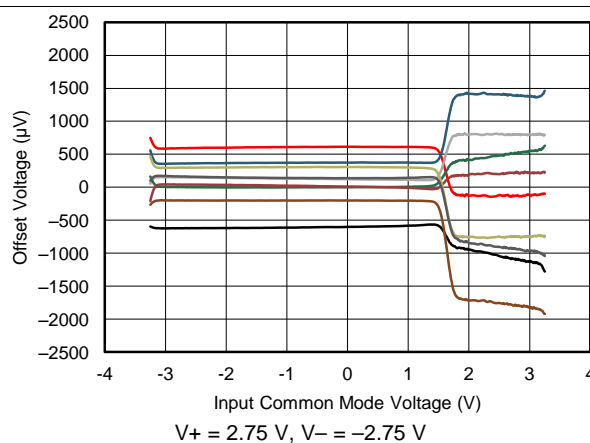


$T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$

**Figure 2. Offset Voltage Drift Distribution**

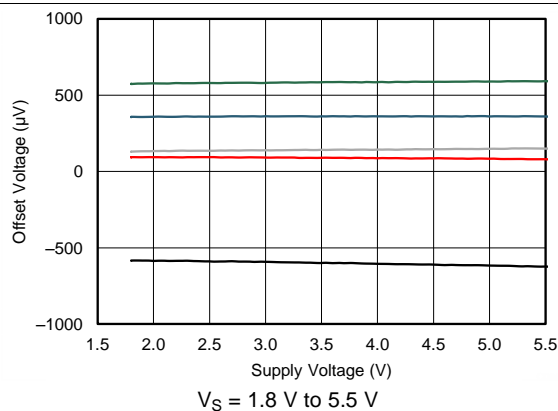


**Figure 3. Offset Voltage vs Temperature**



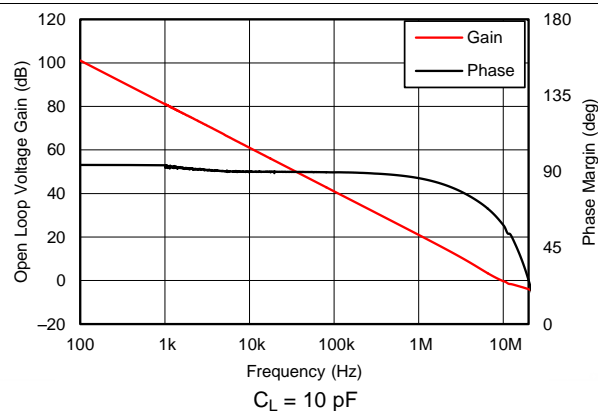
$V_+ = 2.75\text{ V}$ ,  $V_- = -2.75\text{ V}$

**Figure 4. Offset Voltage vs Common-Mode Voltage**



$V_S = 1.8\text{ V}$  to  $5.5\text{ V}$

**Figure 5. Offset Voltage vs Power Supply**

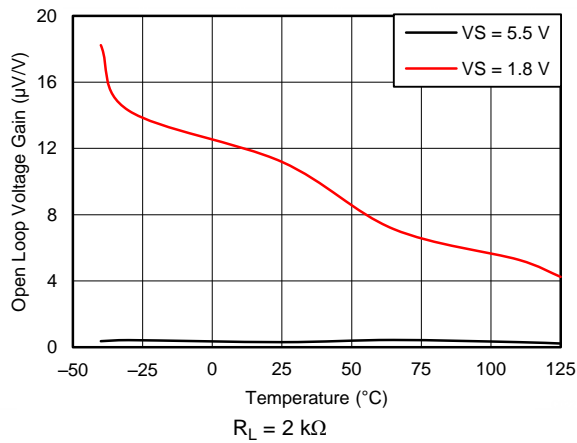


$C_L = 10\text{ pF}$

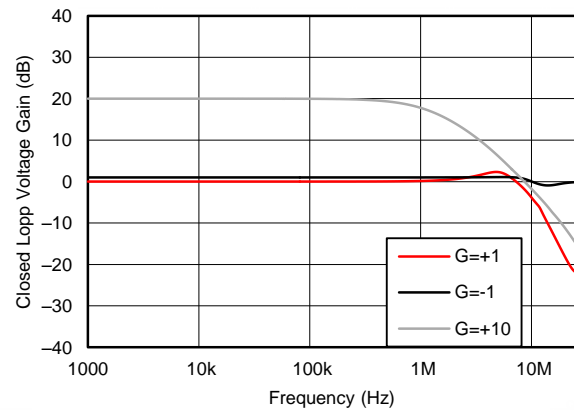
**Figure 6. Open-Loop Gain and Phase vs Frequency**

## Typical Characteristics (continued)

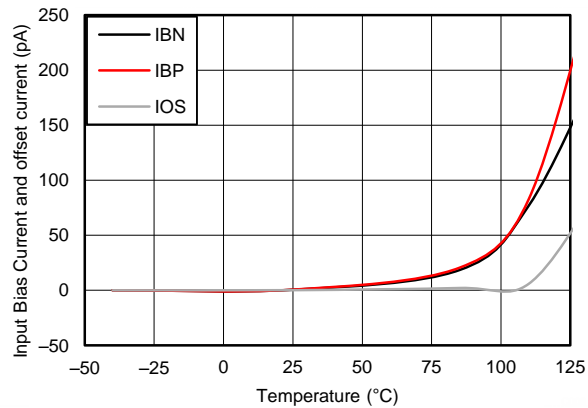
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



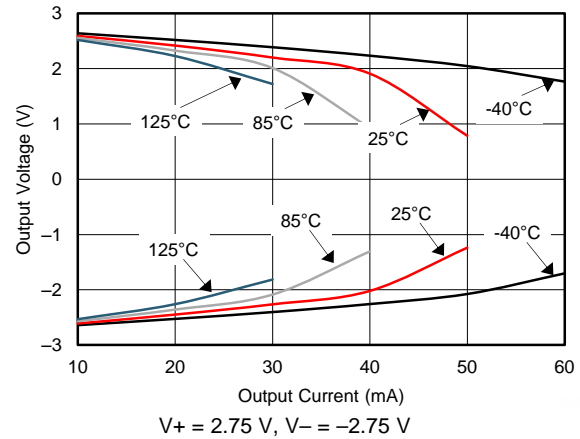
**Figure 7. Open-Loop Gain vs Temperature**



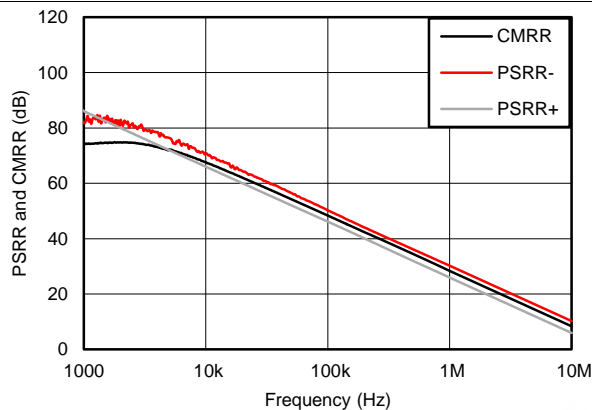
**Figure 8. Closed-Loop Gain vs Frequency**



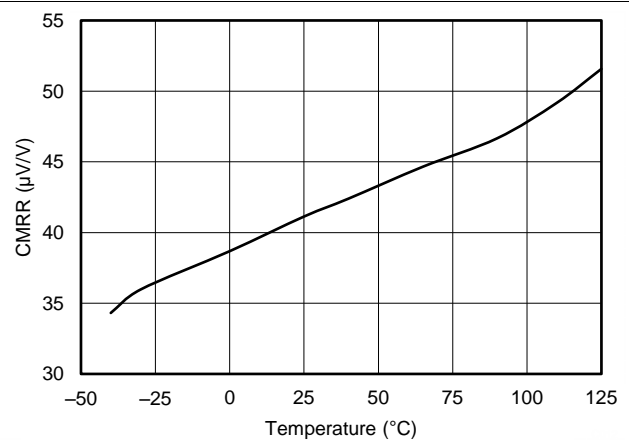
**Figure 9. Input Bias Current vs Temperature**



**Figure 10. Output Voltage Swing vs Output Current**



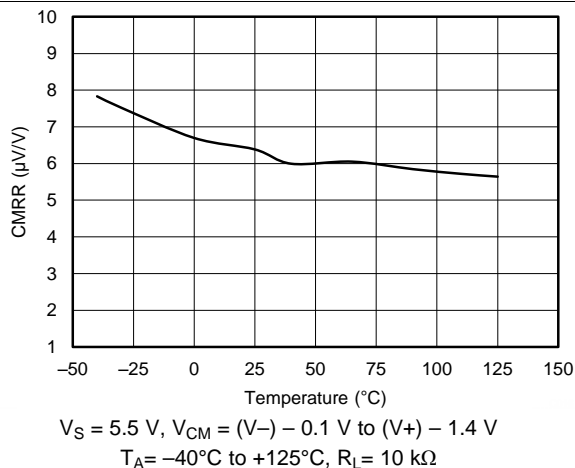
**Figure 11. CMRR and PSRR vs Frequency (Referred to Input)**



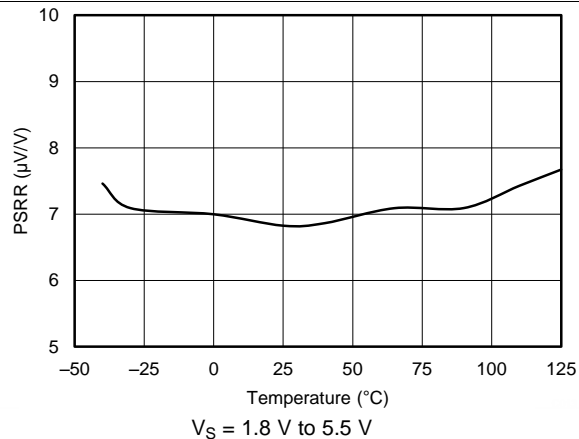
**Figure 12. CMRR vs Temperature**

## Typical Characteristics (continued)

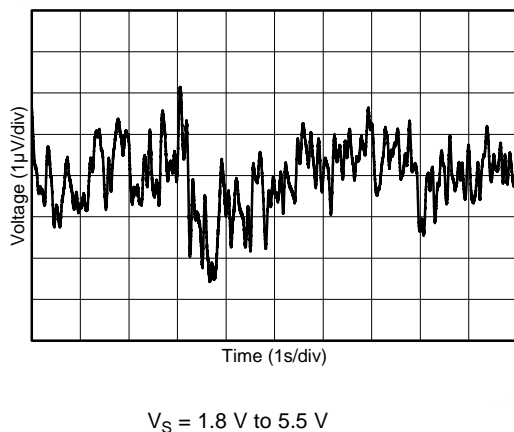
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



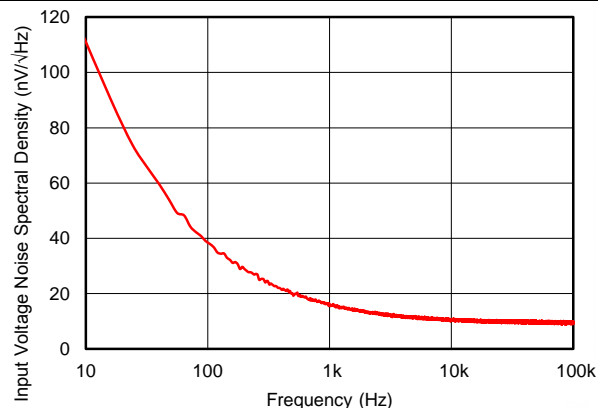
**Figure 13. CMRR vs Temperature**



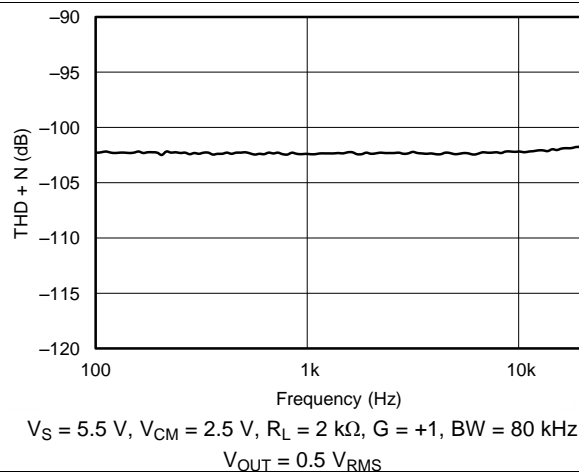
**Figure 14. PSRR vs Temperature**



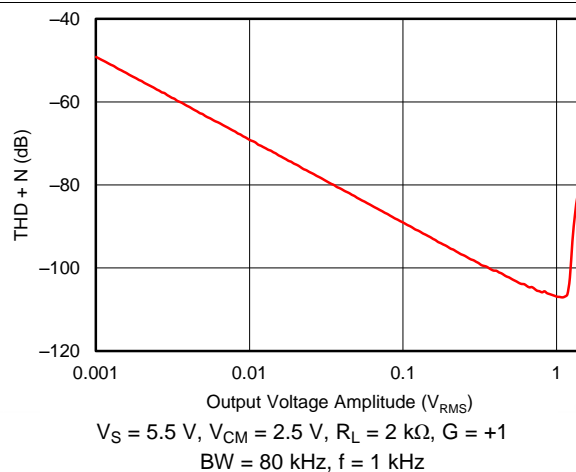
**Figure 15. 0.1-Hz to 10-Hz Input Voltage Noise**



**Figure 16. Input Voltage Noise Spectral Density vs Frequency**



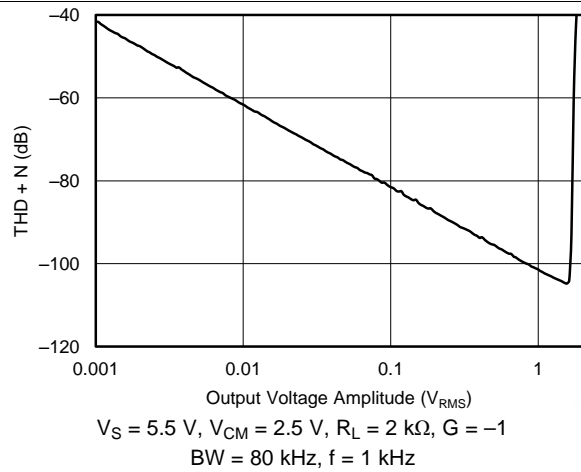
**Figure 17. THD + N vs Frequency**



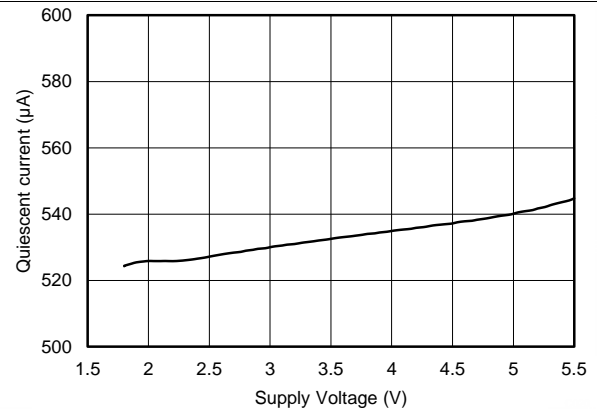
**Figure 18. THD + N vs Amplitude**

## Typical Characteristics (continued)

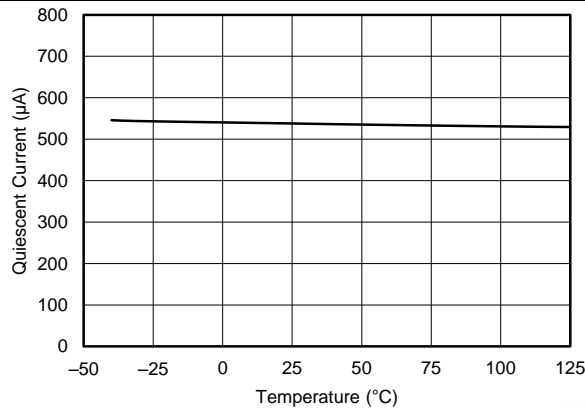
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



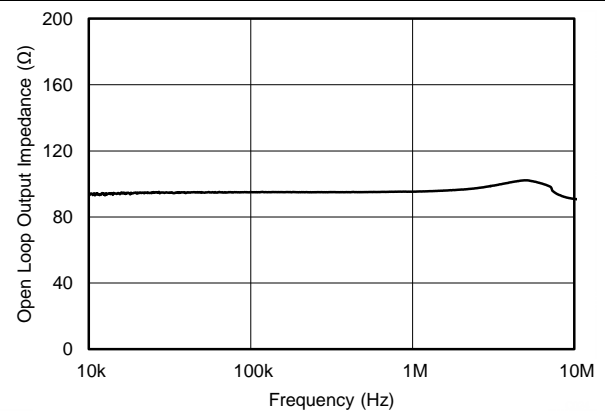
**Figure 19. THD + N vs Amplitude**



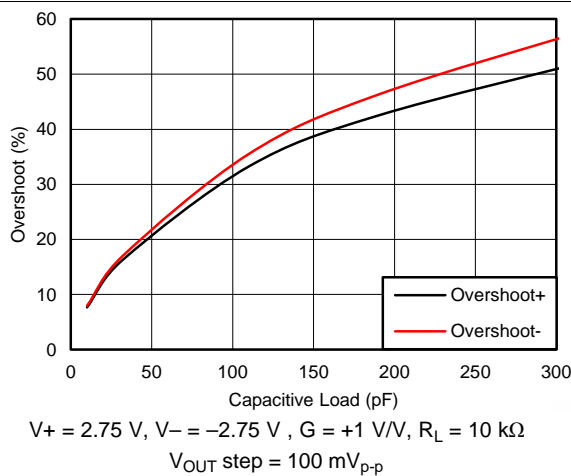
**Figure 20. Quiescent Current vs Supply Voltage**



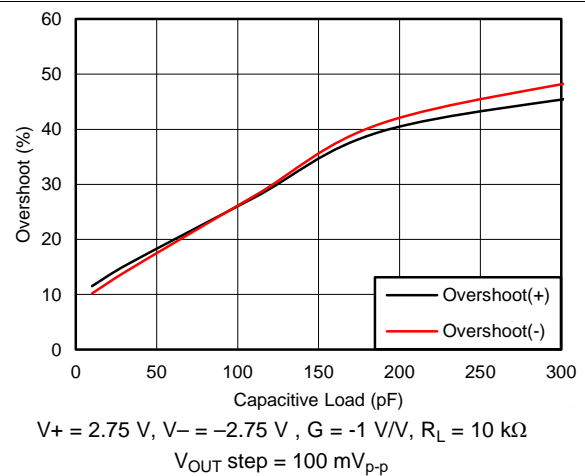
**Figure 21. Quiescent Current vs Temperature**



**Figure 22. Open-Loop Output Impedance vs Frequency**



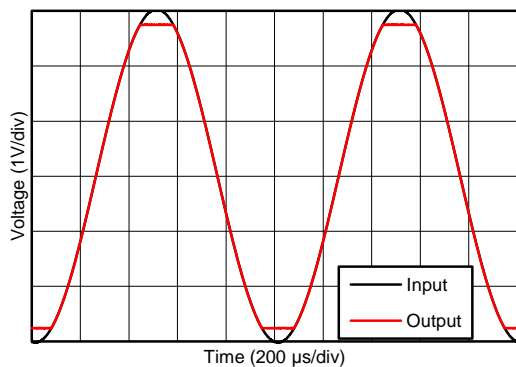
**Figure 23. Small-Signal Overshoot vs Load Capacitance**



**Figure 24. Small-Signal Overshoot vs Load Capacitance**

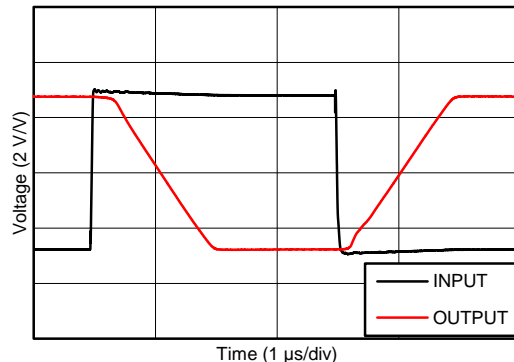
## Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



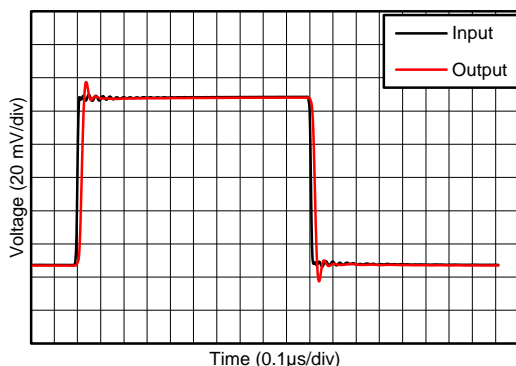
$V_+ = 2.75\text{ V}$ ,  $V_- = -2.75\text{ V}$

**Figure 25. No Phase Reversal**



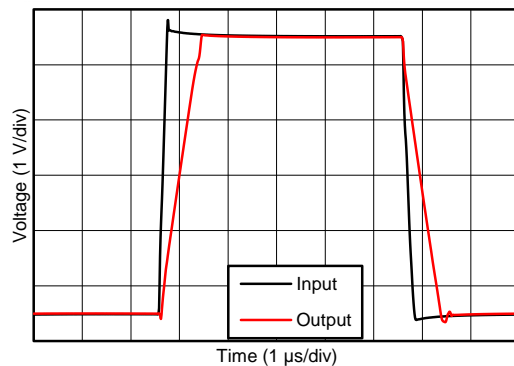
$V_+ = 2.75\text{ V}$ ,  $V_- = -2.75\text{ V}$ ,  $G = -10\text{ V/V}$

**Figure 26. Overload Recovery**



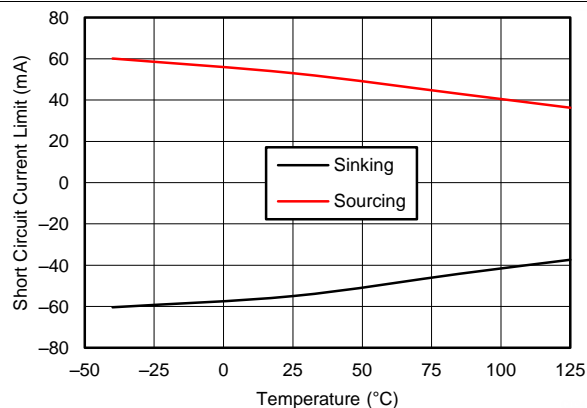
$V_+ = 2.75\text{ V}$ ,  $V_- = -2.75\text{ V}$ ,  $G = 1\text{ V/V}$

**Figure 27. Small-Signal Step Response**

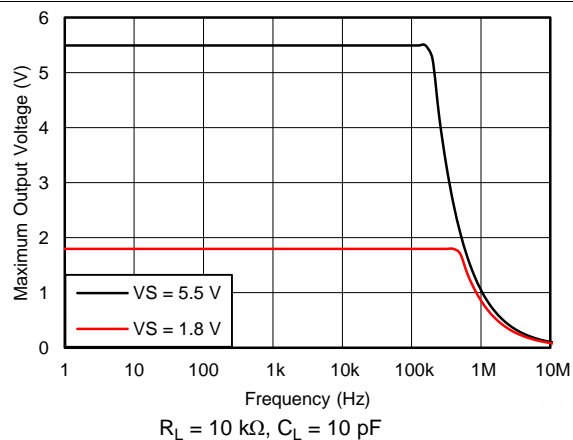


$V_+ = 2.75\text{ V}$ ,  $V_- = -2.75\text{ V}$ ,  $C_L = 100\text{ pF}$ ,  $G = 1\text{ V/V}$

**Figure 28. Large-Signal Step Response**



**Figure 29. Short-Circuit Current vs Temperature**

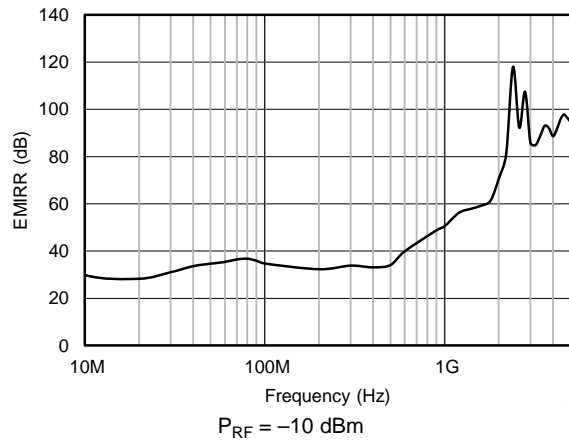


$R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$

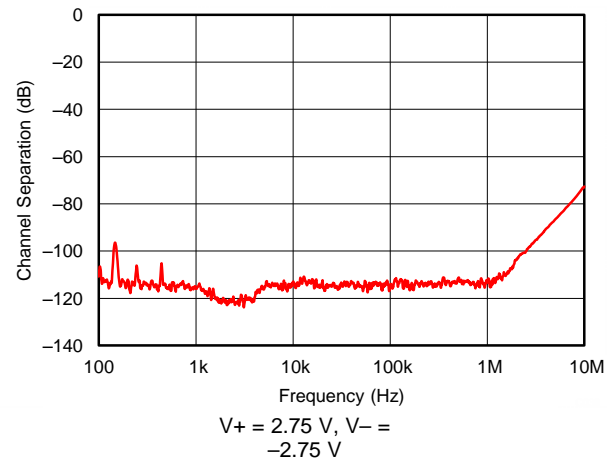
**Figure 30. Maximum Output Voltage vs Frequency and Supply Voltage**

## Typical Characteristics (continued)

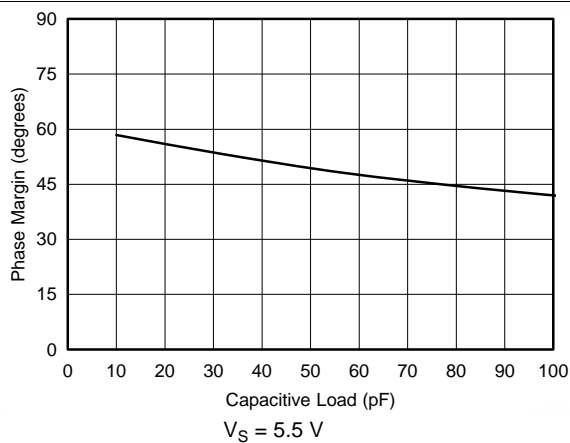
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



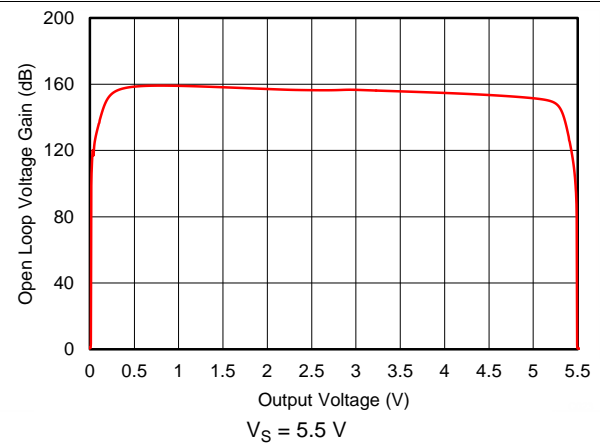
**Figure 31. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency**



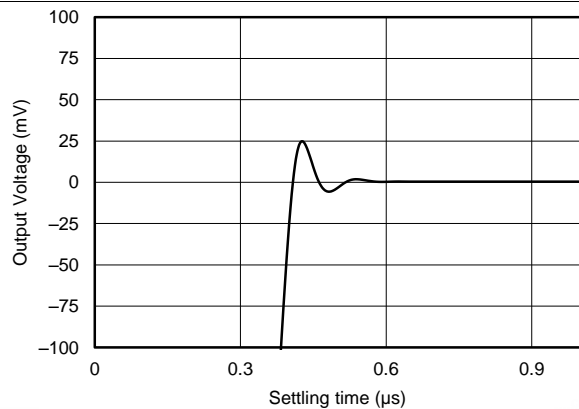
**Figure 32. Channel Separation vs Frequency**



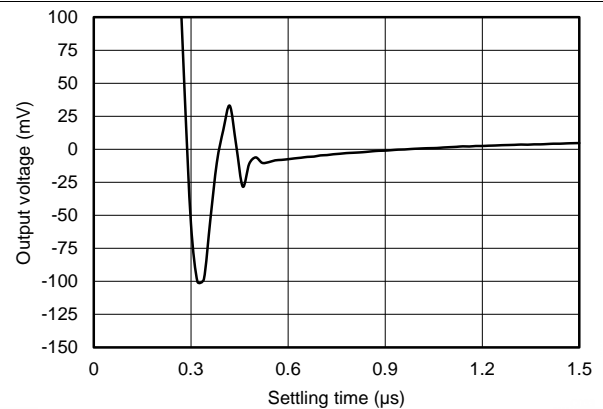
**Figure 33. Phase Margin vs Capacitive Load**



**Figure 34. Open Loop Voltage Gain vs Output Voltage**



**Figure 35. Large Signal Settling Time (Positive)**



**Figure 36. Large Signal Settling Time (Negative)**

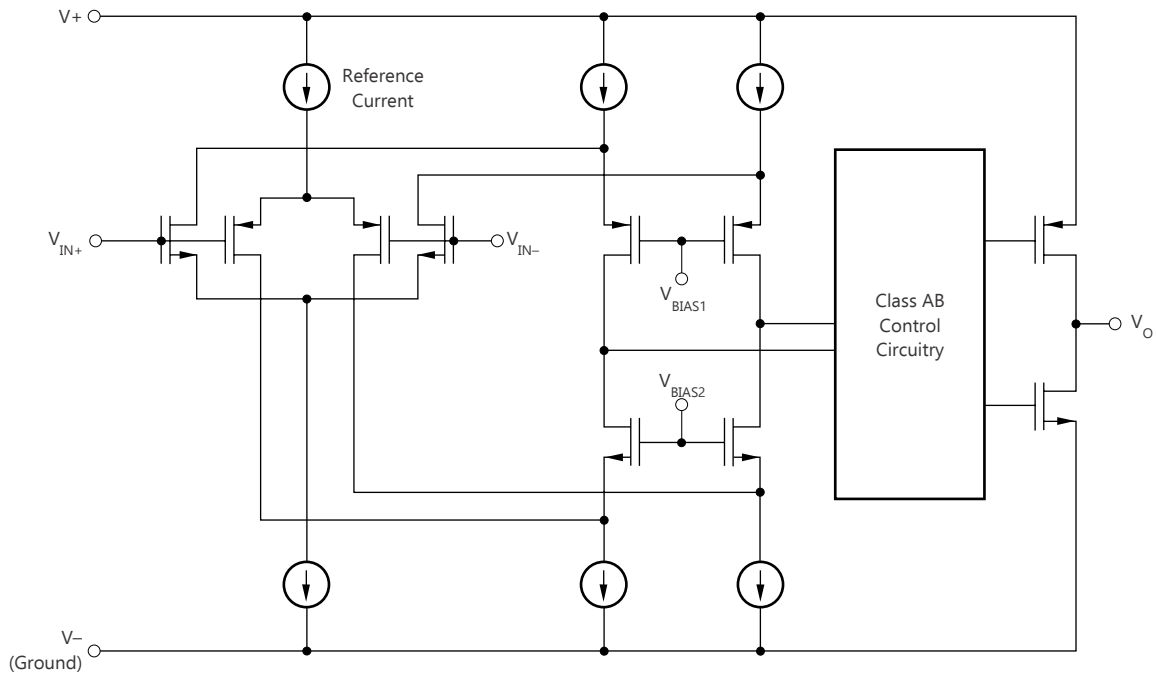


## 9 Detailed Description

### 9.1 Overview

The TLV906x series is a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV906x series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and are designed for driving sampling analog-to-digital converters (ADCs).

### 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TLV906x family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [Functional Block Diagram](#). The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 1.4$  V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately  $(V+) - 1.4$  V. There is a small transition region, typically  $(V+) - 1.2$  V to  $(V+) - 1$  V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from  $(V+) - 1.4$  V to  $(V+) - 1.2$  V on the low end, and up to  $(V+) - 1$  V to  $(V+) - 0.8$  V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

### 9.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV906x series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10-k $\Omega$ , the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

### 9.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV906x series is approximately 200 ns.

## 9.4 Device Functional Modes

The TLV906x family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V ( $\pm 0.9$  V) and 5.5 V ( $\pm 2.75$  V).

## 10 Application and Implementation

### NOTE

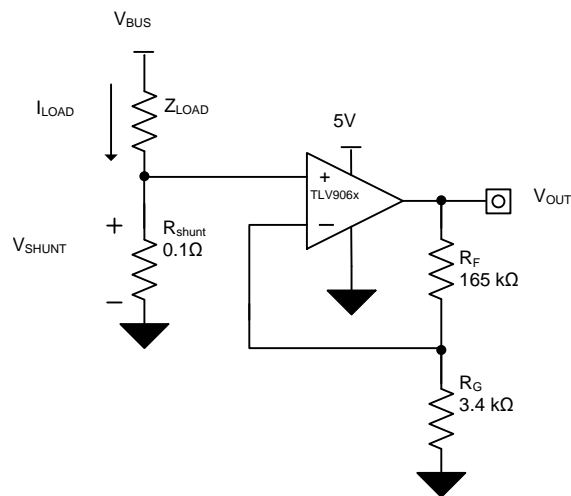
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The TLV906x series features 10-MHz bandwidth and 6.5-V/ $\mu$ s slew rate with only 538- $\mu$ A of supply current per channel, providing good ac performance at very-low-power consumption. DC applications are well served with a very-low input noise voltage of 10 nV /  $\sqrt{\text{Hz}}$  at 10 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

### 10.2 Typical Application

Figure 37 shows the TLV906x configured in a low-side current sensing application.



**Figure 37. TLV906x in a Low-Side, Current-Sensing Application**

#### 10.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

## Typical Application (continued)

### 10.2.2 Detailed Design Procedure

The transfer function of the circuit in [Figure 37](#) is given in [Equation 1](#)

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current ( $I_{LOAD}$ ) produces a voltage drop across the shunt resistor ( $R_{SHUNT}$ ). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using [Equation 2](#).

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

Using [Equation 2](#),  $R_{SHUNT}$  equals 100 m $\Omega$ . The voltage drop produced by  $I_{LOAD}$  and  $R_{SHUNT}$  is amplified by the TLV906x to produce an output voltage of approximately 0 V to 4.95 V. [Equation 3](#) calculates the gain required for the TLV906x to produce the required output voltage.

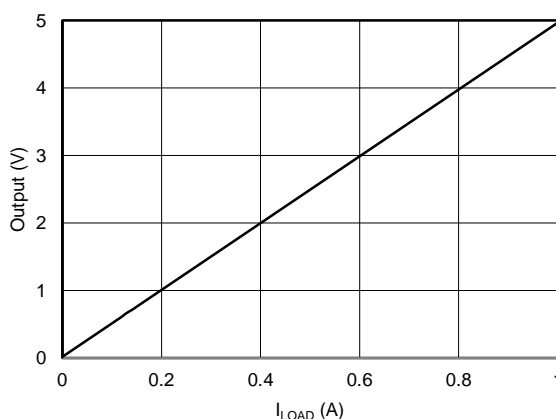
$$\text{Gain} = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using [Equation 3](#), the required gain equals 49.5 V/V, which is set with the  $R_F$  and  $R_G$  resistors. [Equation 4](#) sizes the  $R_F$  and  $R_G$  resistors to set the gain of the TLV906x to 49.5 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting  $R_F$  to equal 165 k $\Omega$  and  $R_G$  to equal 3.4 k $\Omega$  provides a combination that equals approximately 49.5 V/V. [Figure 38](#) shows the measured transfer function of the circuit shown in [Figure 37](#).

### 10.2.3 Application Curve



**Figure 38. Low-Side, Current-Sense, Transfer Function**

## 11 Power Supply Recommendations

The TLV906x series is specified for operation from 1.8 V to 5.5 V ( $\pm 0.9$  V to  $\pm 2.75$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

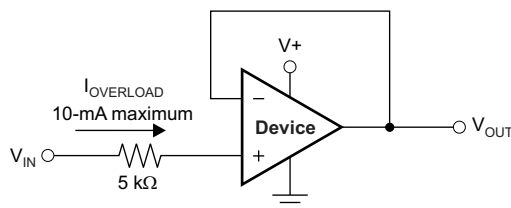
### CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the [Absolute Maximum Ratings](#) table.

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the section.

### 11.1 Input and ESD Protection

The TLV906x series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as shown in the [Absolute Maximum Ratings](#) table. [Figure 39](#) shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.



**Figure 39. Input Current Protection**

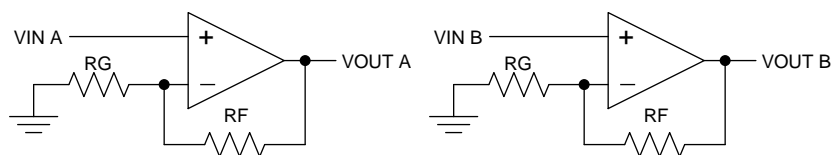
## 12 Layout

### 12.1 Layout Guidelines

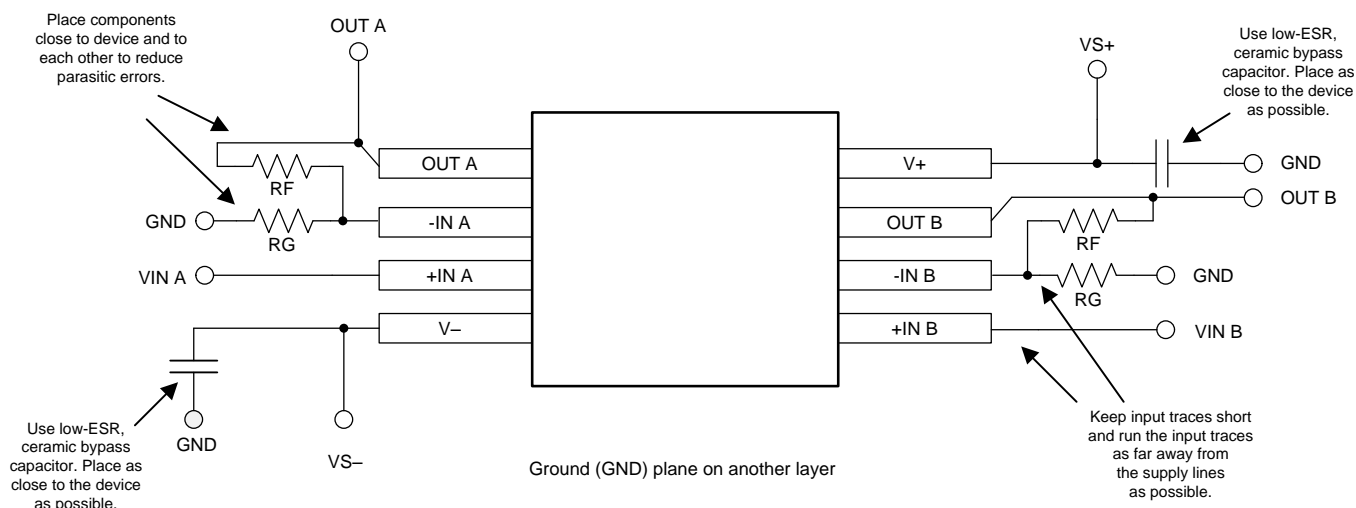
For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 41](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

## 12.2 Layout Example



**Figure 40. Schematic Representation for Figure 41**



**Figure 41. Layout Example**

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

Texas Instruments, [TLVx313 Low-Power, Rail-to-Rail In/Out, 500- \$\mu\$ V Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems](#).

Texas Instruments, [TLVx314 3-MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier](#).

Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers](#).

Texas Instruments, [QFN/SON PCB Attachment](#).

Texas Instruments, [Quad Flatpack No-Lead Logic Packages](#).

Texas Instruments, [Circuit Board Layout Techniques](#).

Texas Instruments, [Single-Ended Input to Differential Output Conversion Circuit Reference Design](#).

### 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV9061	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TLV9062	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TLV9064	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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### 13.5 Trademarks

E2E is a trademark of Texas Instruments.

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### 13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



## 13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV90611DPWR	ACTIVE	X2SON	DPW	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	CG	<a href="#">Samples</a>
TLV90621DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T062	<a href="#">Samples</a>
TLV90621DGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T062	<a href="#">Samples</a>
TLV90621DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TL9062	<a href="#">Samples</a>
TLV90621DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T062	<a href="#">Samples</a>
TLV90621DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T062	<a href="#">Samples</a>
TLV90621PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TL9062	<a href="#">Samples</a>
TLV90641DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9064D	<a href="#">Samples</a>
TLV90641PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TLV9064	<a href="#">Samples</a>
TLV90641PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TLV9064	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

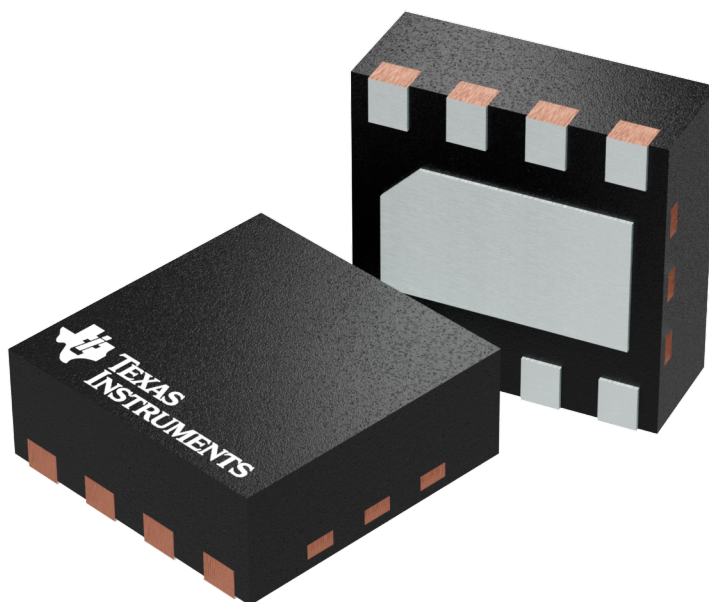
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9061IDPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9062IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9062IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9062IDR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062IDSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9062IDSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9062IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9064IDR	SOIC	D	14	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9064IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9064IPWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS

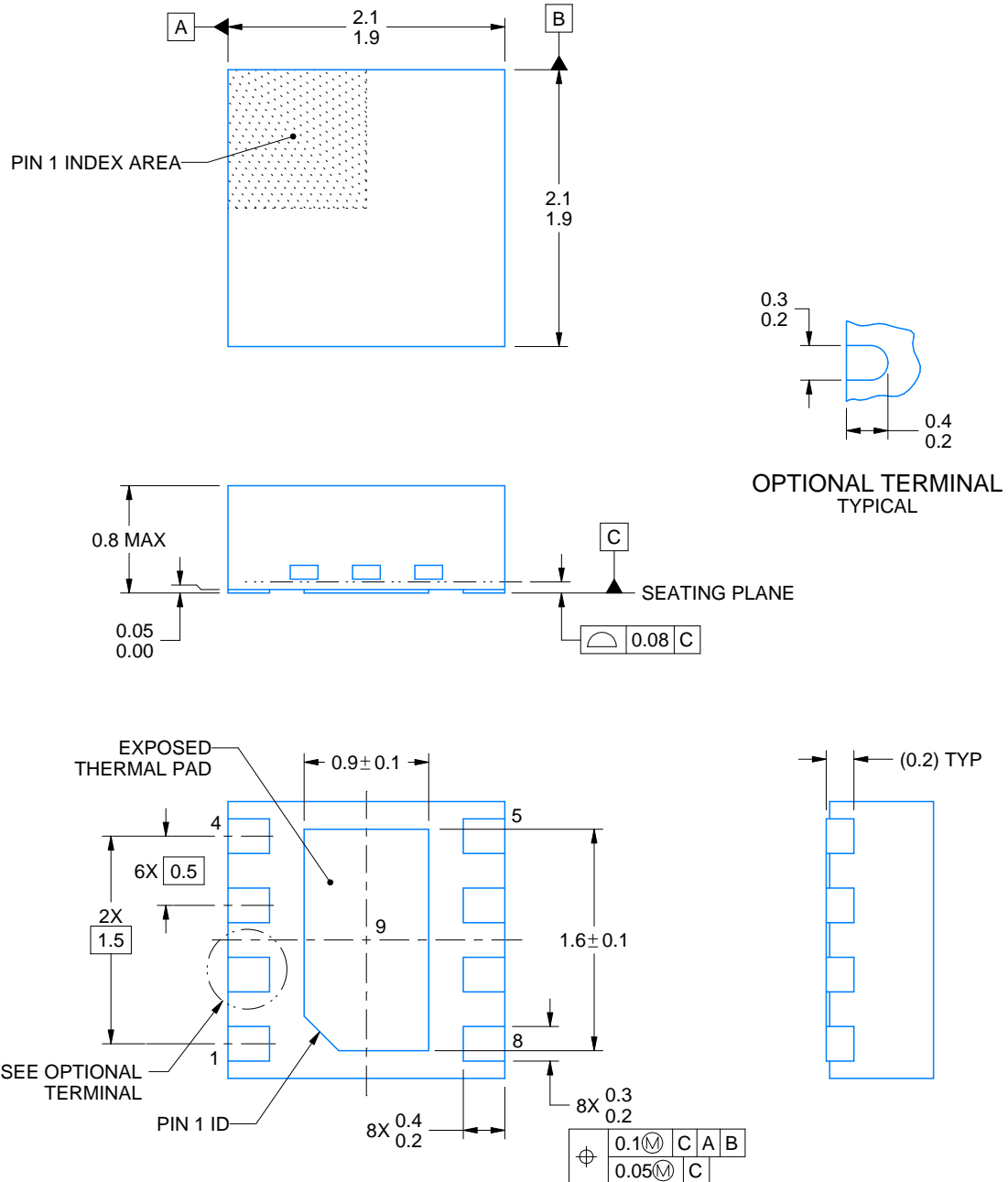
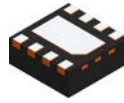


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9061IDPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV9062IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9062IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TLV9062IDR	SOIC	D	8	2500	333.2	345.9	28.6
TLV9062IDSGR	WSO	DSG	8	3000	210.0	185.0	35.0
TLV9062IDSGT	WSO	DSG	8	250	210.0	185.0	35.0
TLV9062IPWR	TSSOP	PW	8	2000	366.0	364.0	50.0
TLV9064IDR	SOIC	D	14	2500	336.6	336.6	41.3
TLV9064IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
TLV9064IPWT	TSSOP	PW	14	250	366.0	364.0	50.0



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4218900/B 09/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



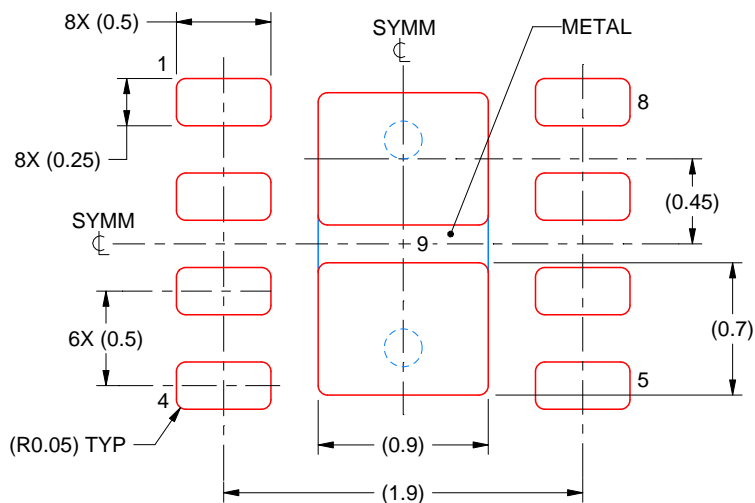


## EXAMPLE STENCIL DESIGN

DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4218900/B 09/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

**DPW 5**

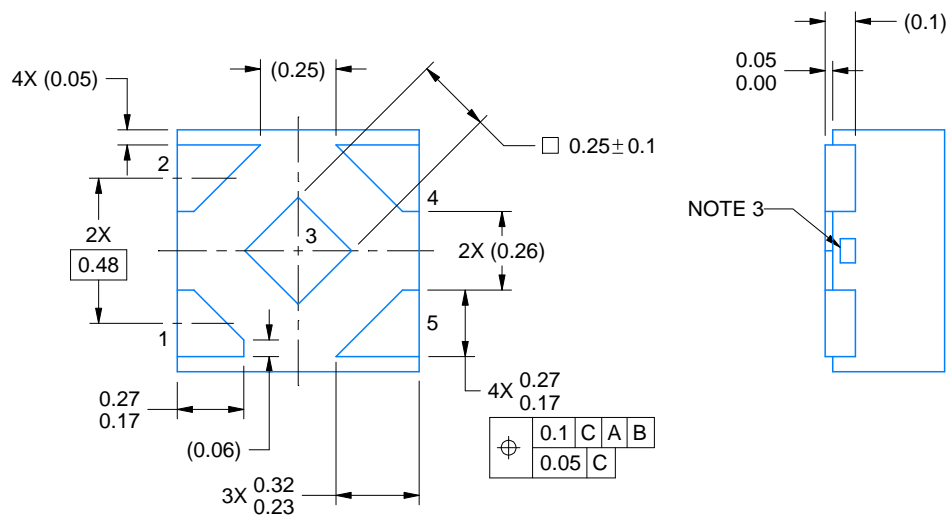
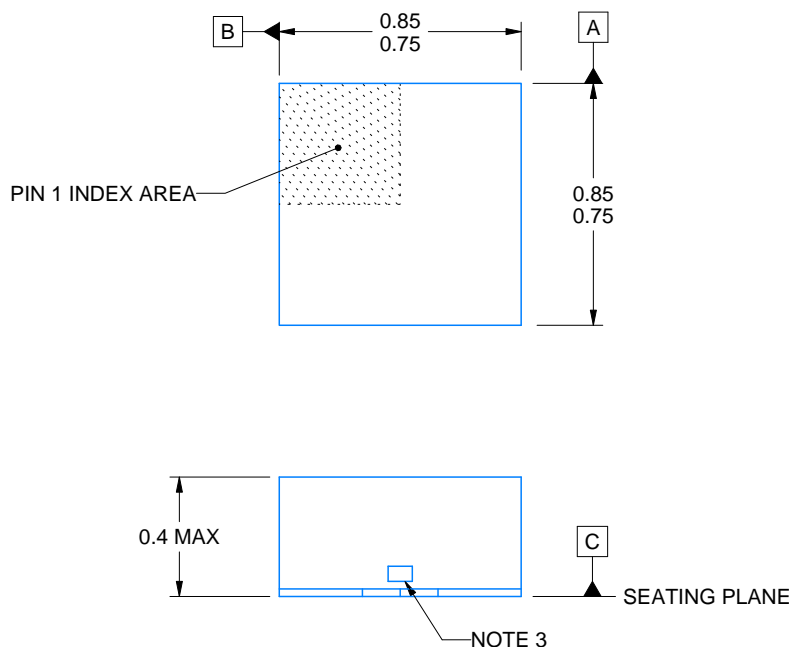
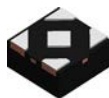
**X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211218-3/D



4223102/B 09/2017

## NOTES:

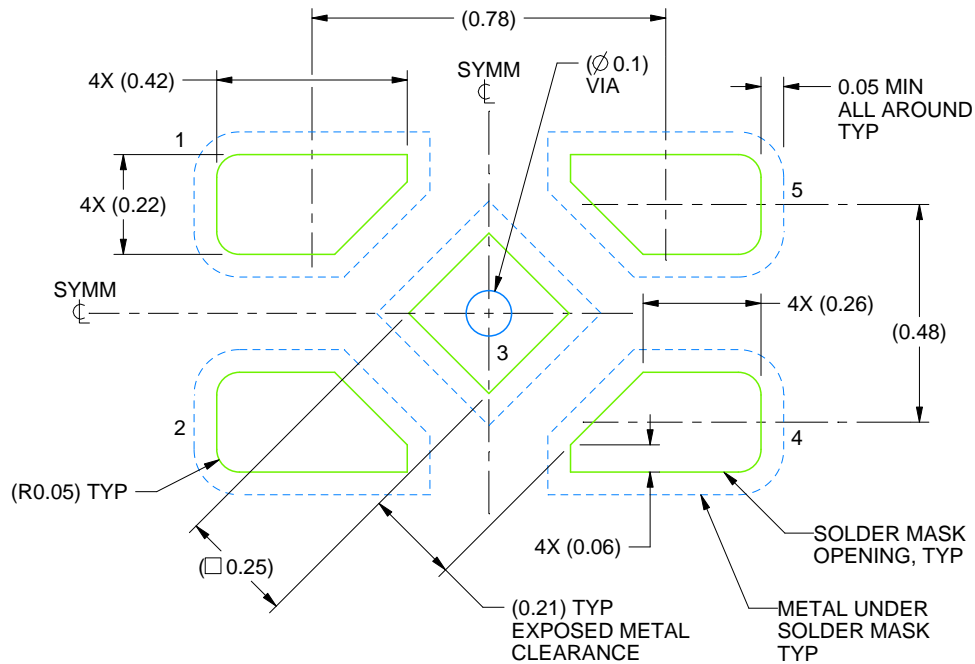
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

# EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:60X

4223102/B 09/2017

NOTES: (continued)

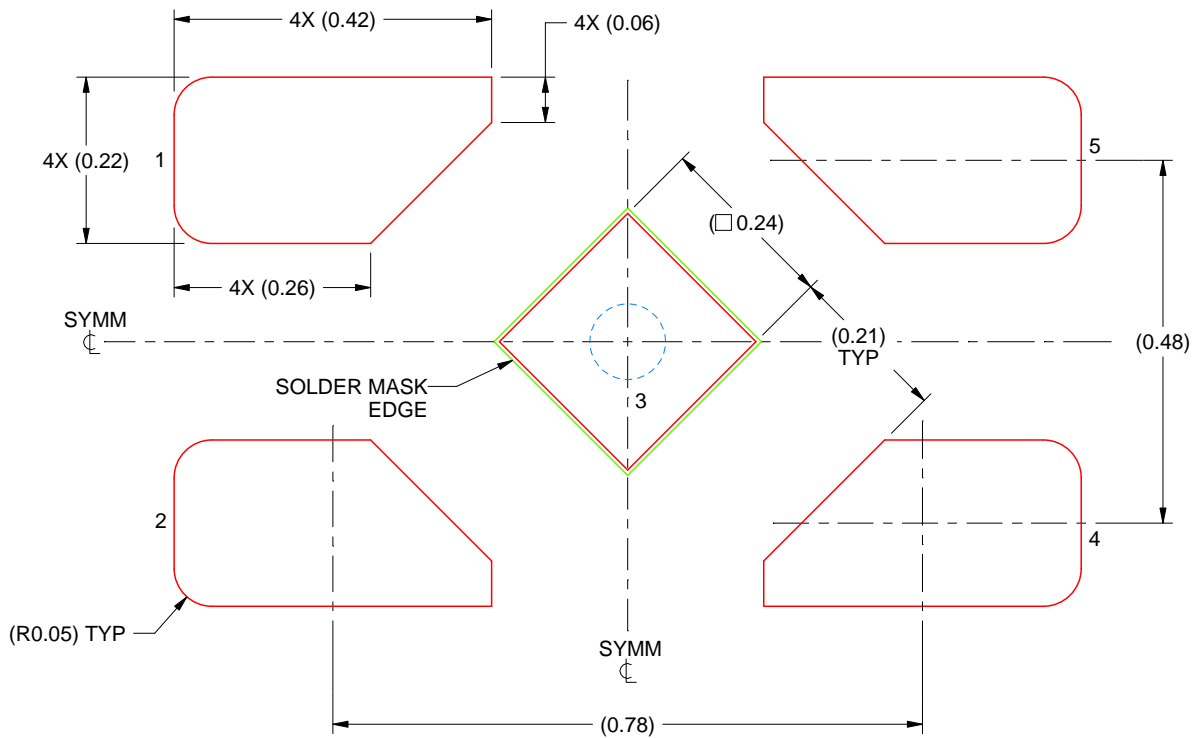
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD  
92% PRINTED SOLDER COVERAGE BY AREA  
SCALE:100X

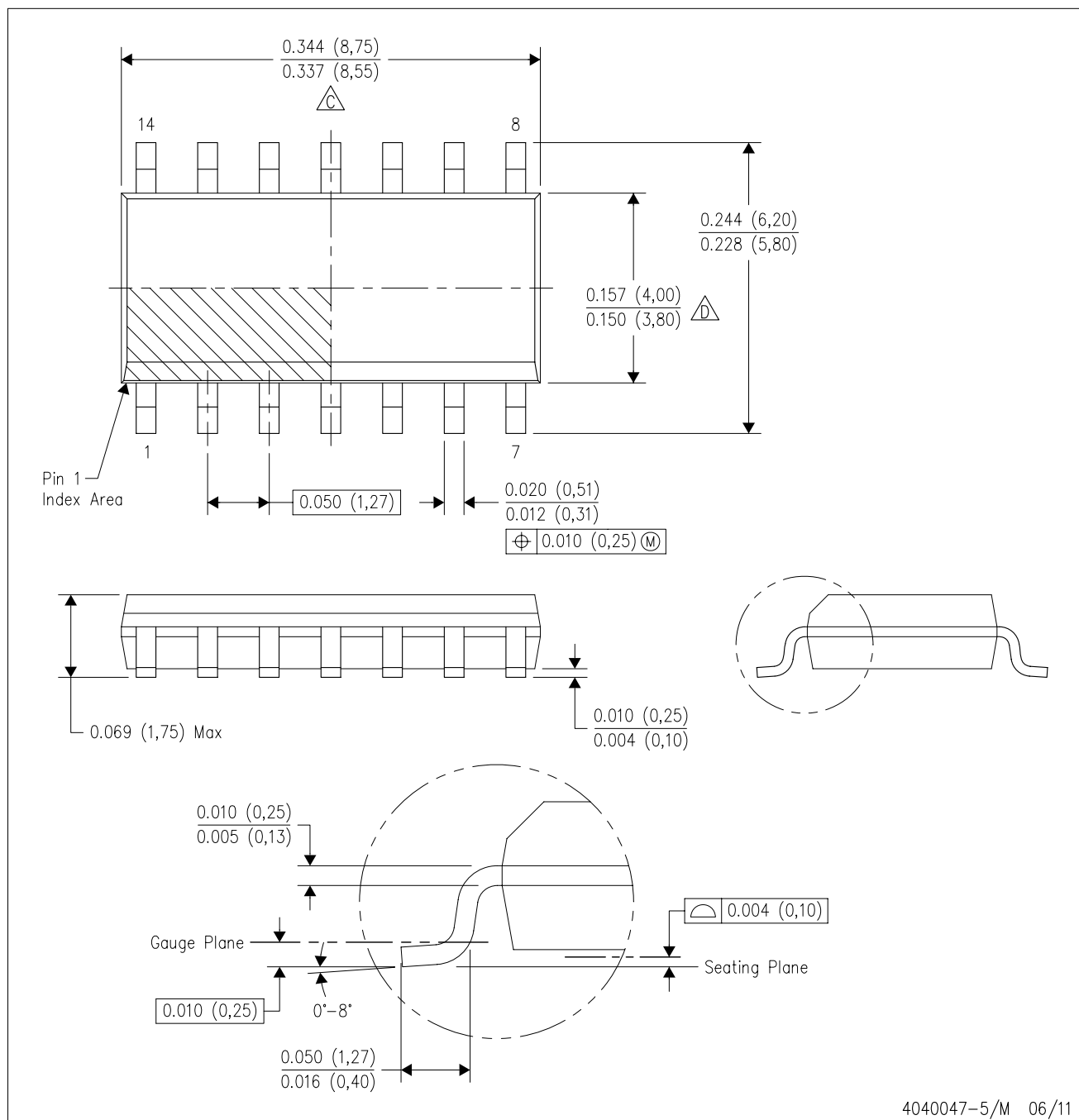
4223102/B 09/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

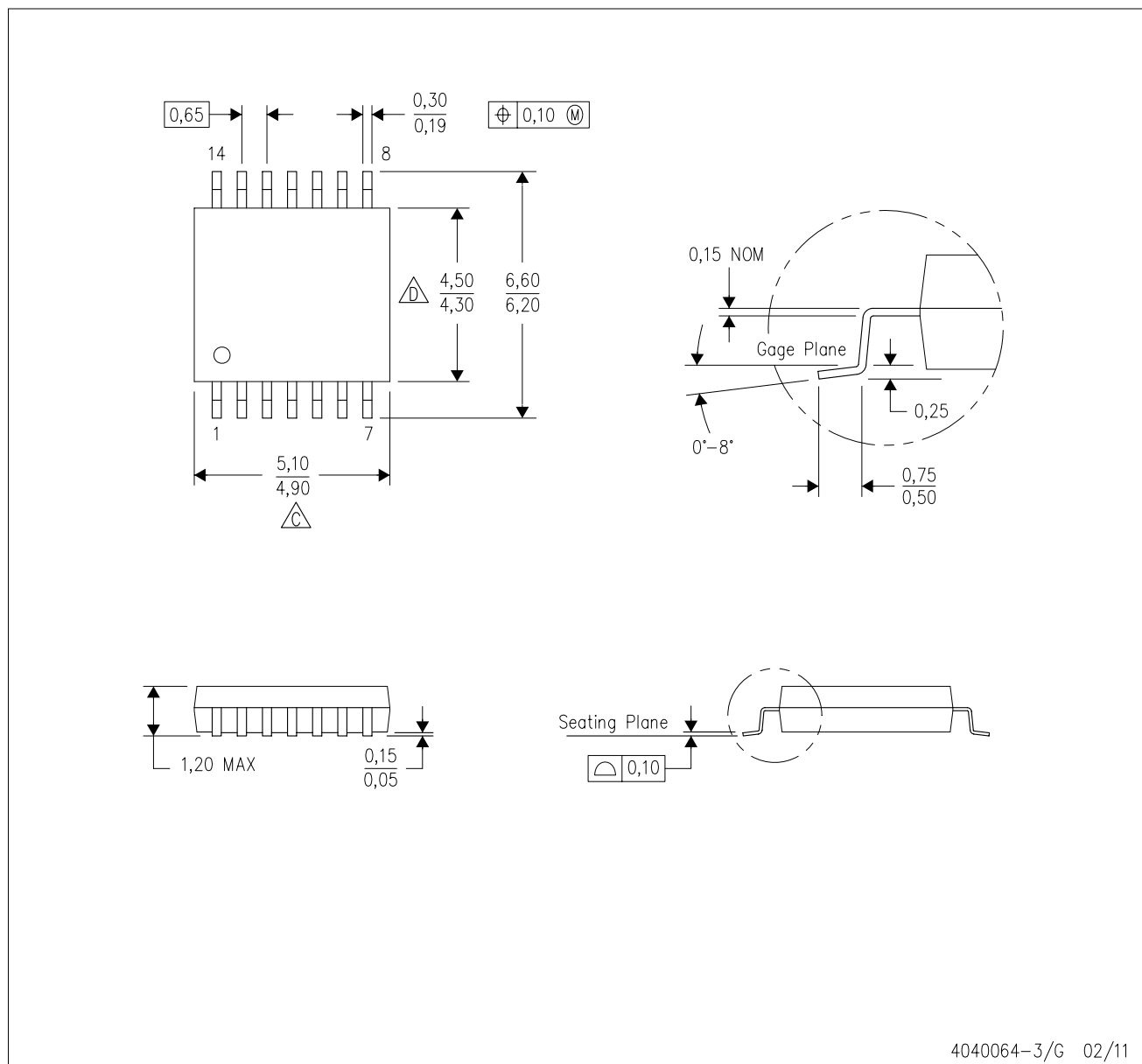


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

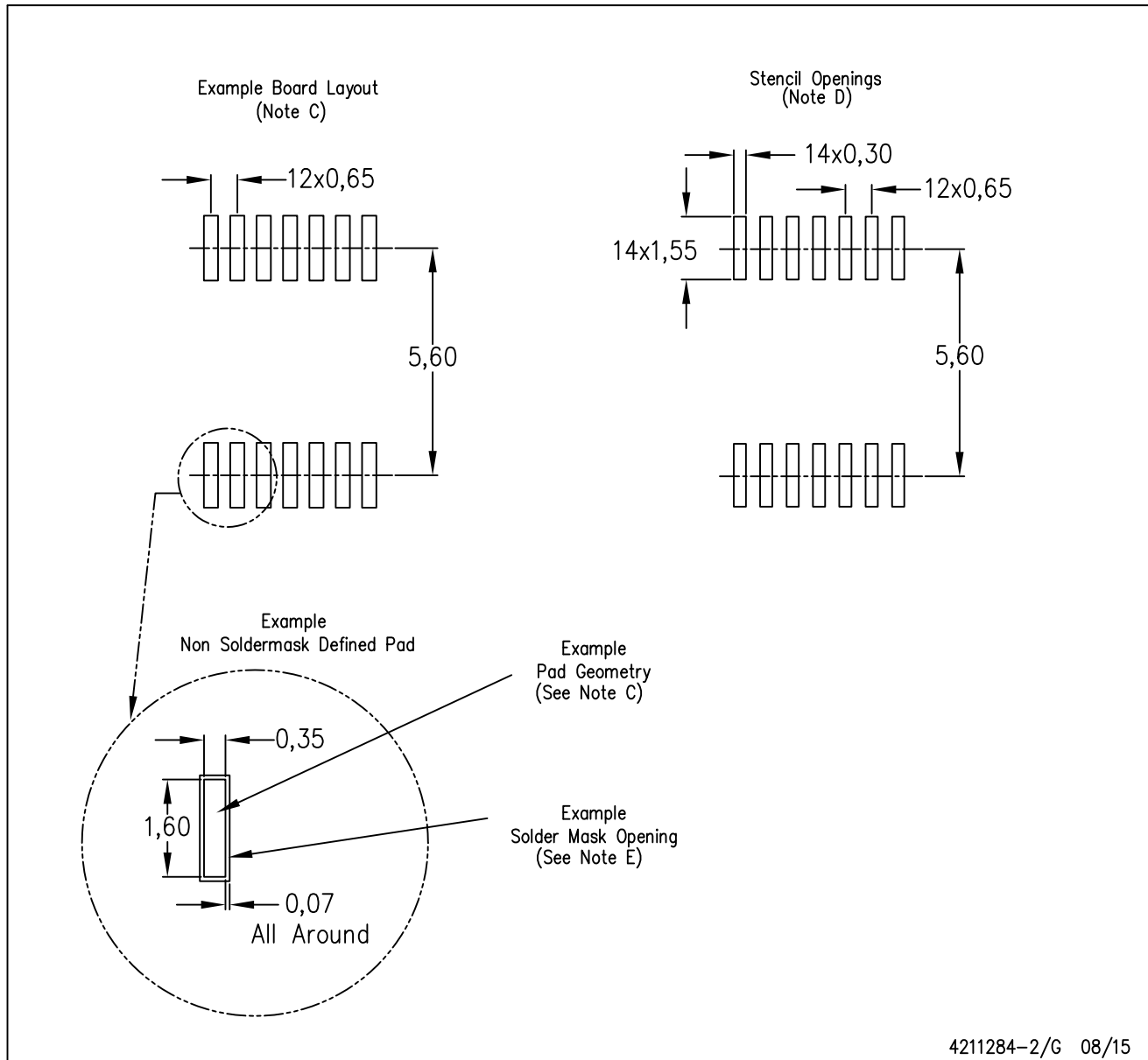
PLASTIC SMALL OUTLINE



4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

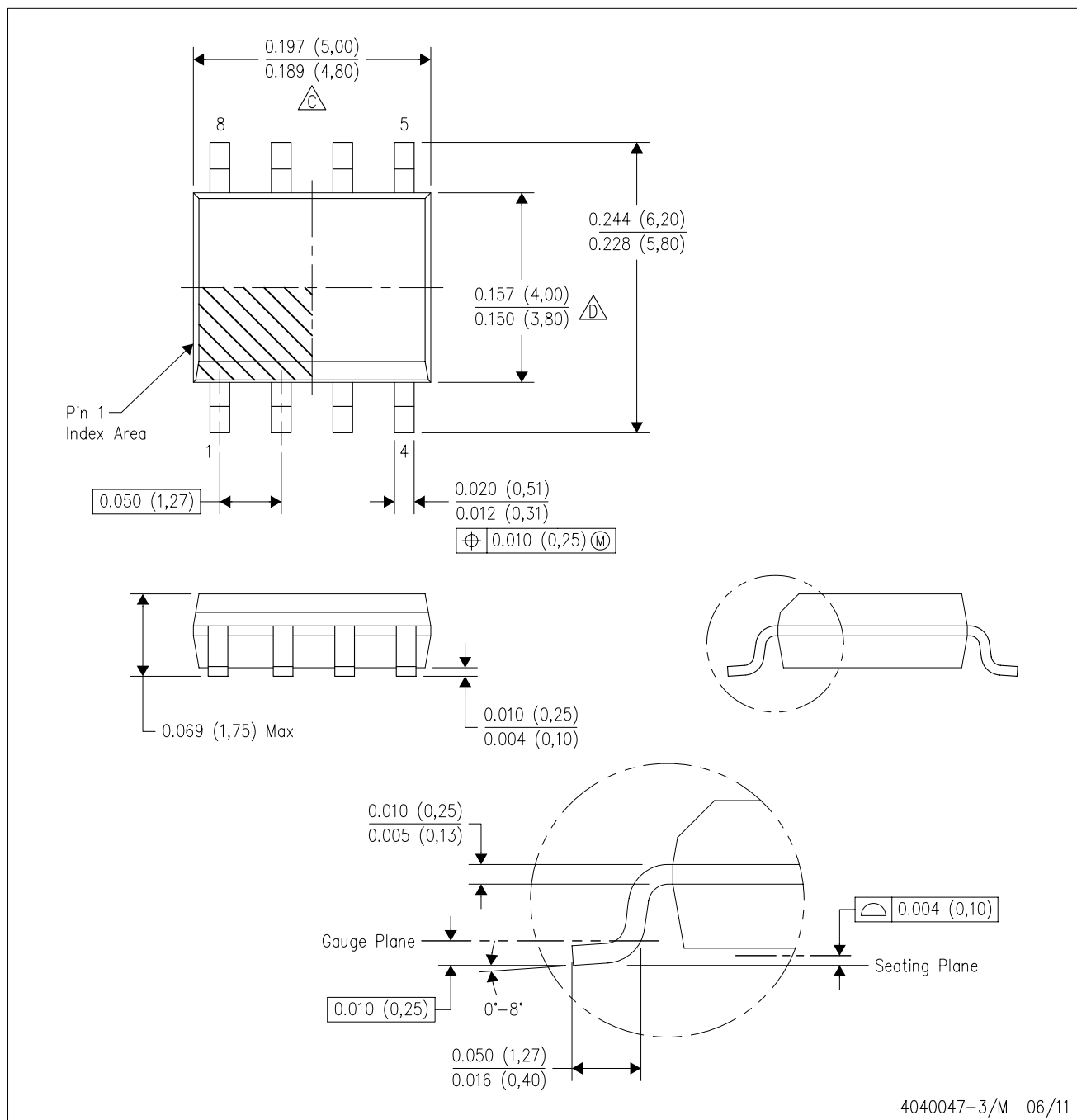


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

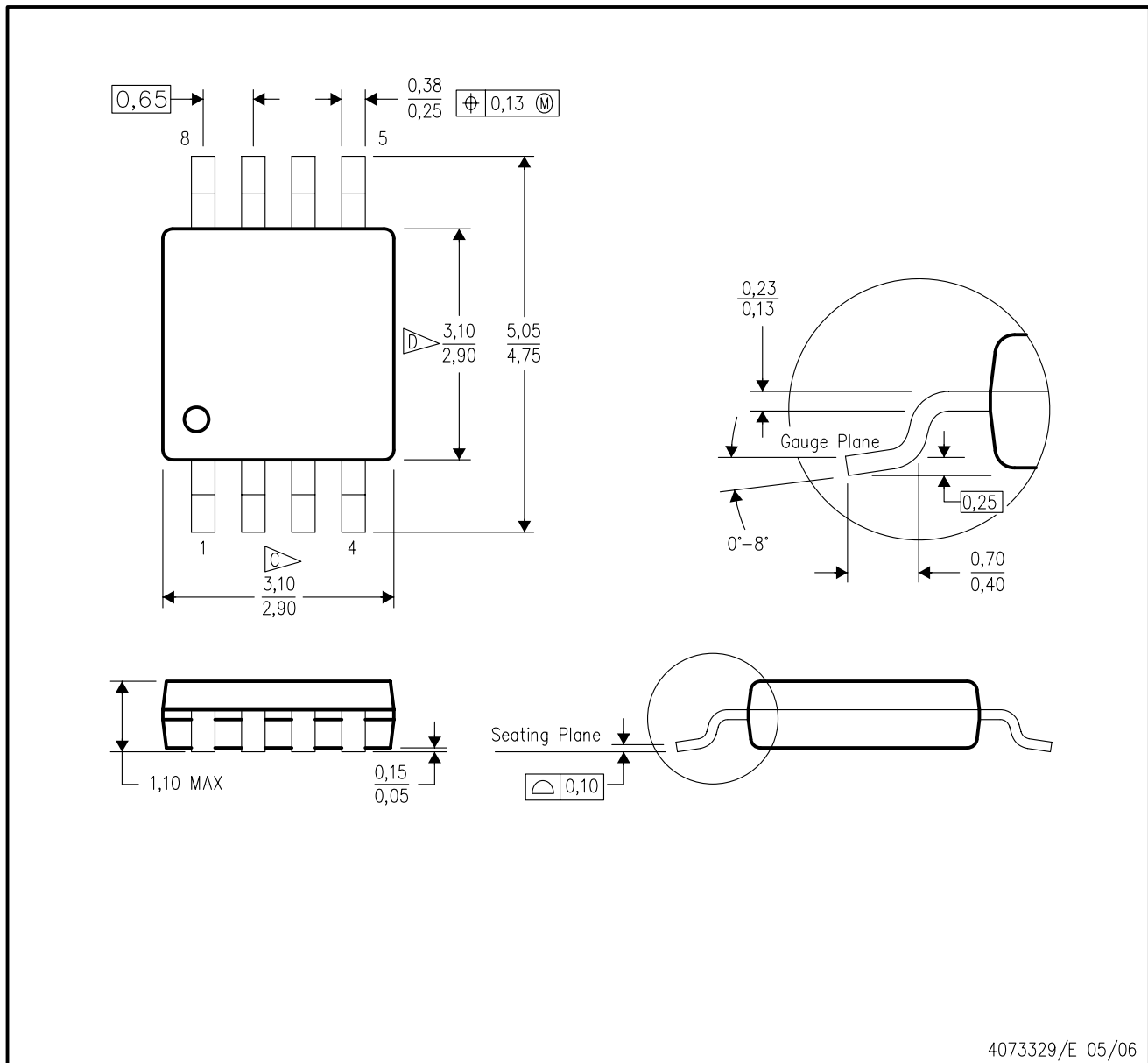


## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

DGK (S-PDSO-G8)

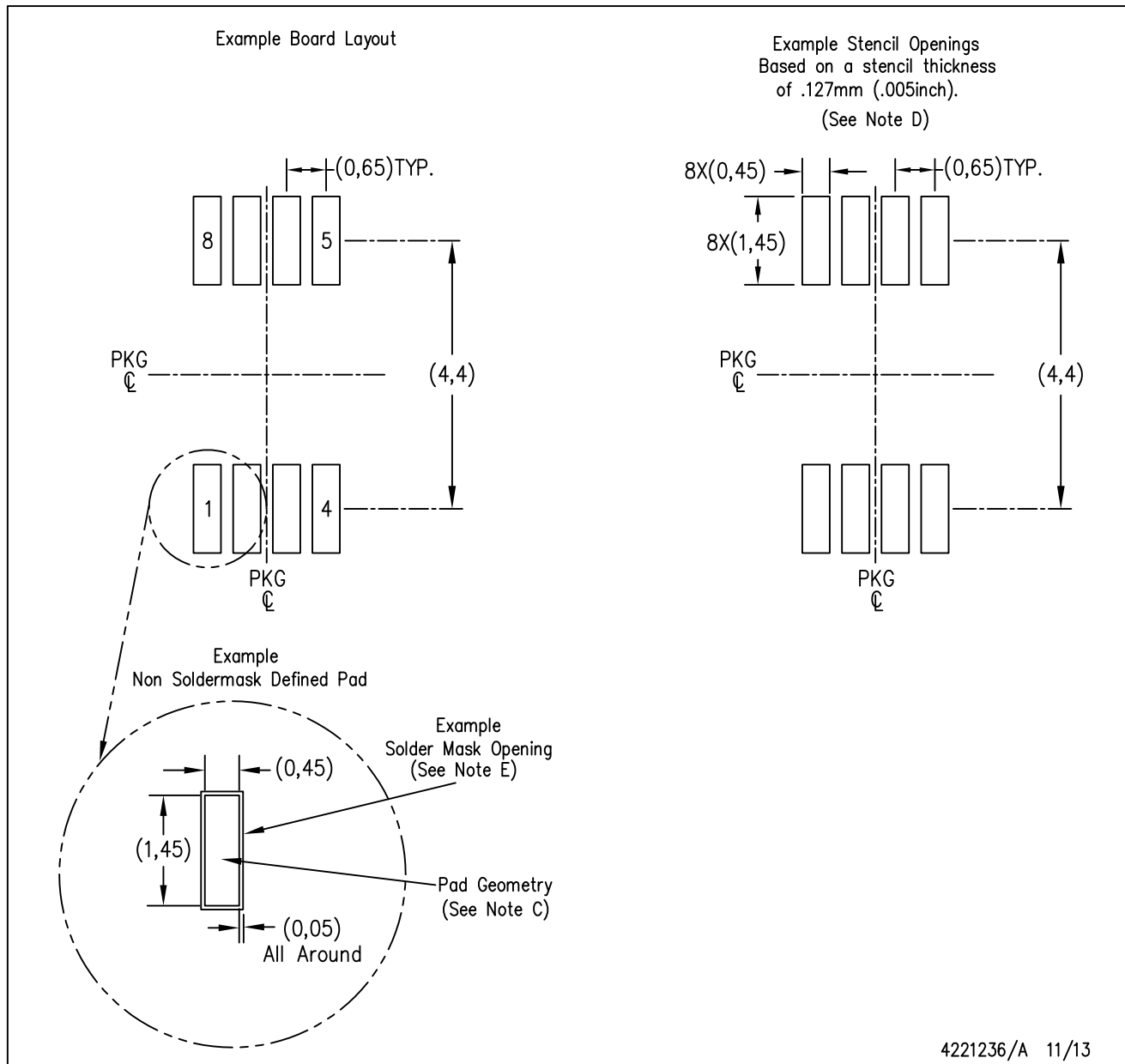
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

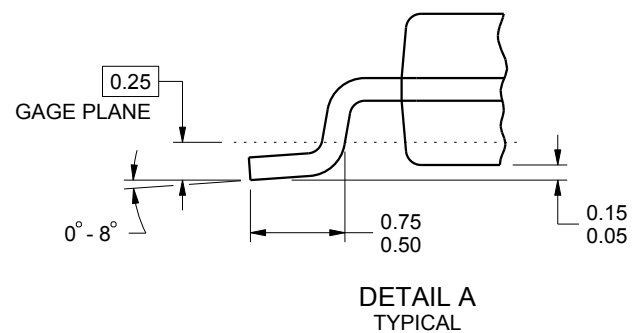
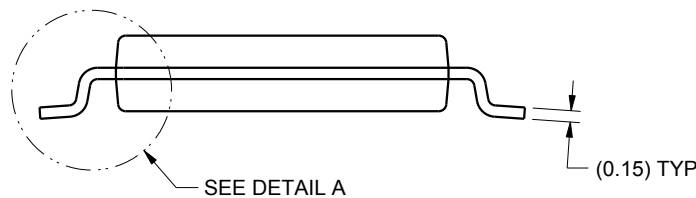
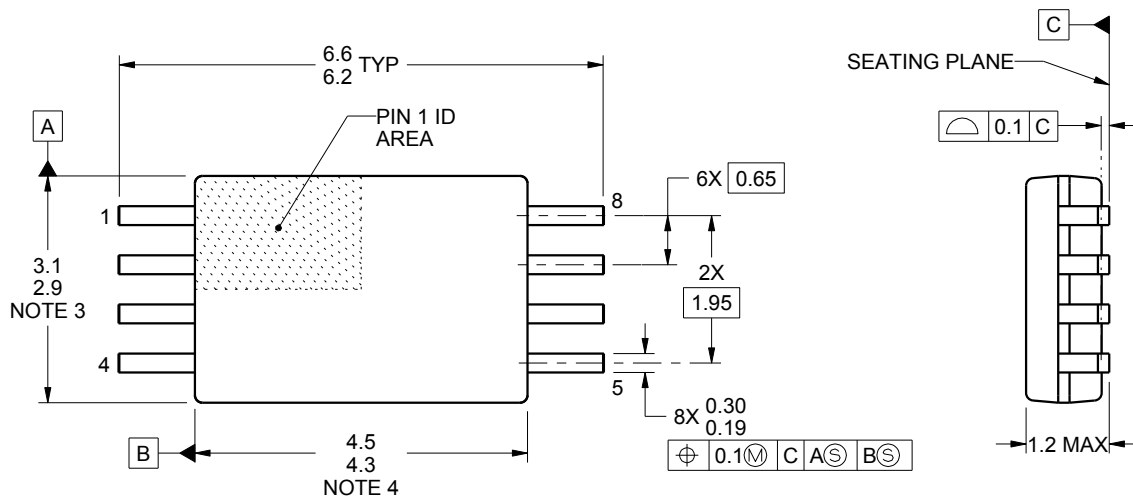
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

### NOTES:

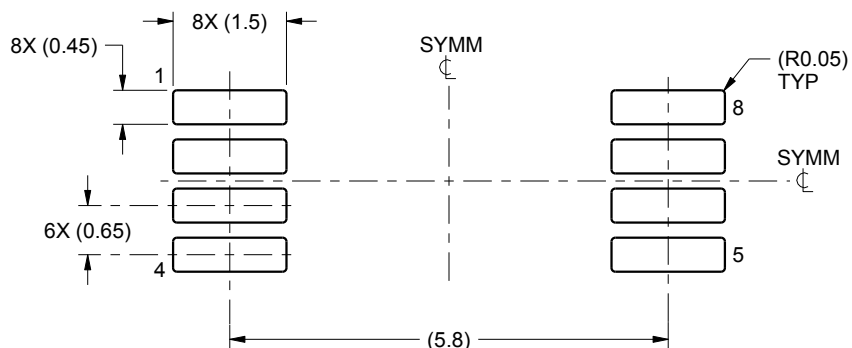
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

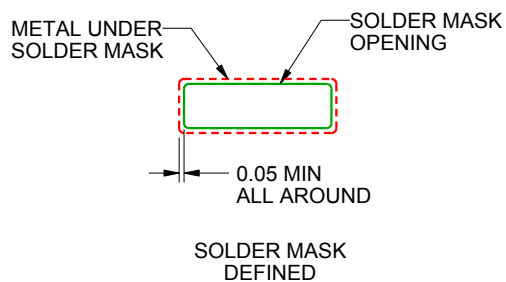
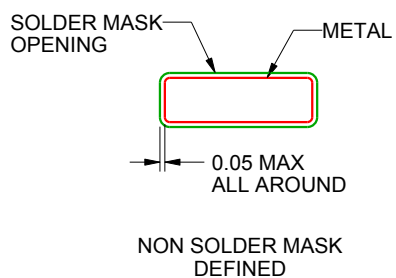
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

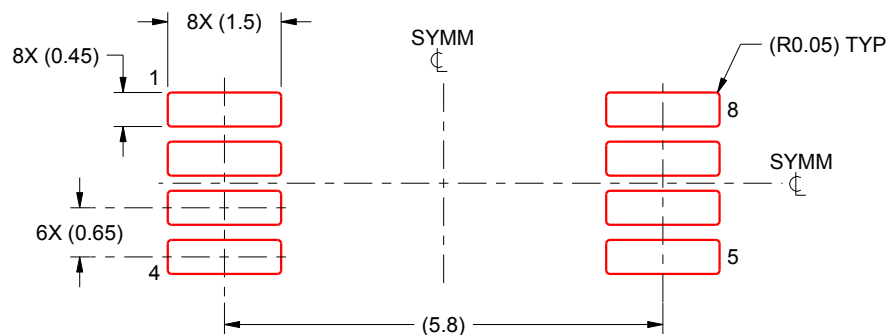
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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